

Operating long on-chip buses

The present invention relates to operating long on-chip buses.

Integrating large system on chip (SOC) devices can be a great challenge as the
5 environment on the chip becomes more and more noisy. At the same time as the technology
shrinks, on-chip wires are becoming narrower and denser, and their RC time constants are
increasing. This leads to worsening delay over long interconnect runs. Such delays call for
techniques which will enable on-chip buses to run at highest possible speed allowed by the
environment.

10 Typically, inverters or buffers are used as receivers at the receiving end of a
bus. Figure 1 of the accompanying drawings schematically illustrates a bus on an integrated
circuit device, the bus including a series of bus lines 4 which are interconnecting wires
between drivers 2 and receivers 6. Each bus line 4 connects a driver 2 to a corresponding
receiver 6. Since the rise/fall times are typically excessively long (for example, see figure 2
15 of the accompanying drawings; "IN" refers to input to bus driver and "LINEOUT" refers to
output at the end of a 10mm long bus on Metal 2 CMOS12) at the receiving end, the speed of
sensing transitions on the bus is very slow, if the switching threshold of the inverter/buffer
receiver is at $V_{dd}/2$ (half the supply voltage).

20 It is proposed to change this threshold (lower/raise) for both the rising and
falling edge transitions so as to achieve fast sensing as well as achieve robust signaling in
noisy environment. Changing the thresholds may cause the receiver to sense glitches caused
by crosstalk, which are highly undesirable. In the case of very noisy environment the
25 threshold can be raised above $V_{dd}/2$. Thus there exists a possibility to vary threshold of the
receiver in order to achieve robust signaling at the highest possible speed in that
environment.

Schmitt triggers are often used for rejecting noise wherein hysteresis of the
transfer characteristics is utilized to raise the threshold for rising transitions and vice-versa

for falling transitions at its input. However, this only provides variation of threshold in one direction and cannot be calibrated. In the proposed scheme the threshold can be varied in both the directions (raise or lower from $V_{dd}/2$ point) to suit the conditions on the chip. Since the calibration is done on the chip it takes care of process variations on both the front-end
5 processing as well as on the backend processing.

According to one aspect of the present invention, there is provided a bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that each receiver circuit comprises:

- 10 - a first detector (10) operably connected to receive a data signal from an associated bus line (4), and operable to detect a rising transition of the data signal with respect to a first threshold level, and to produce a first output signal upon detection of such a rising transition;
- a second detector (12) operably connected to receive the data signal, and
15 operable to detect a falling transition of the data signal with respect to a second threshold level, and to produce a second output signal upon detection of such a transition; and
- output means operable to output the first or second output signal as a receiver output signal.

According to another aspect of the present invention, there is provided a
20 method of operating a bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that the method comprises:

- receiving a data signal from a bus line (4);
- detecting a rising or falling transition of the data signal with respect to first
25 and second threshold levels respectively;
- producing a first output signal upon detection of a rising transition, or producing a second output signal upon detection of a falling transition; and
outputting the first or second output signal as a receiver output signal.

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Figure 1 illustrates schematically a bus on an integrated circuit device;

Figure 2 illustrates RC response at the receiving end of a 10mm wire on an M2,0.13 μ m CMOS circuit;

Figure 3 illustrates a receiver circuit;

Figure 4 illustrates the receiver circuit of Figure 3 in more detail;

Figure 5 illustrates a scheme with a dummy bus;

Figure 6 illustrates a scheme which uses the same bus for calibration;

Figure 7 illustrates a state diagram for the calibration circuit;

5 Figure 8 illustrates glitch detection by using convention latches;

Figure 9 illustrates some of the simulation waveforms.

Figure 3 illustrates a receiver circuit for use in embodiments of the present
 10 invention. The receiver of Figure 3 has first and second detectors 10 and 12. The first
 detector 10 is sensitive to transitions occurring from low to high and the second detector from
 high to low. Both detectors are connected to receive the data signal transmitted on the bus
 wire 4, and are operable to detect respective transitions of that signal on the bus wire 4. The
 detectors have respective outputs which are combined via a multiplexer 14. The multiplexer
 15 14 has a select line controlled by the previous data on the bus wire 4. The previous data value
 is stored in a state element 16. A state element could be a flip-flop, latch or a delay line.

The thresholds of the first and second detectors of the receiver are controlled
 by a control word, which is generated by a calibrator (not shown in Figure 3).

The receiver circuit is shown in more detail in Figure 4. It consists of two
 20 inverters whose thresholds can be controlled independently by the calibrator. The calibrator
 applies the control word, which selects the number of transistors T10, T12 to be used in
 parallel in a respective pull down/up networks in the inverters of the receiver. This tunes the
 threshold of the inverters for rising and falling transitions respectively. The selection of
 signal to be output from the multiplexer is based on the previous value of the output, which is
 25 stored in the state element 16. For example, if the present value is high then the multiplexer
 14 selects the output of the detector (inverter) 12 which is sensitive to falling transitions.

The calibrator 18 uses either a dummy bus as shown in Figure 5, or the main
 bus with slight modifications in the driver circuit (which then uses a multiplexer) as shown in
 Figure 6, to simulate worst case switching conditions on the chip. The simulation enables the
 30 calibrator to set the control word to an appropriate value. The calibration can be done once
 during power-up or during chip initialization. The dummy bus 20 technique shown in Figure
 5 involves the use of an extra set of bus drivers 22, bus lines 24, and bus receivers 26 to
 simulate the cross talk to be executed on the real bus 2,4,6.

The calibrator circuit is preferably implemented as a finite state machine (shown in Figure 7), which applies signals on primary bus wires (aggressor wires) and measures the crosstalk on at least one secondary bus wire (victim wire). If a glitch is detected which can possibly cause failure then it changes the threshold of the receiver 10, 12 and re-applies the signals to the primary bus wires. This procedure is repeated until the output of the receiver circuit.

A glitch sensor circuit 28, which includes a pair of latches, is used to capture the glitches. See Figure 8. The first latch 30, is transparent low and is connected to 'b' in Figure 4. The other latch 32 is transparent high and is connected to 'a' in Figure 4. Output from one of the latch is selected by a multiplexer 34 based on the logic level on the victim wire M which is generated by the calibrator 18.

Figure 7 illustrates the state diagram of the calibrator, 'M' and 'S' represent the signals on victim and aggressor wires respectively. Calibration starts when 'Ca' is asserted. 'T' is the reset signal to the glitch capturing latches. 'C' is a signal which goes high whenever the latches detect appreciable glitch at their inputs. 'CW1' and 'CW2' are the signals which are used to increment a counter in the calibrator 18 that generates the control word for the receiver circuit threshold adaptation.

As the calibration proceeds it can be seen with reference to Figure 9 that the thresholds of the receiving inverters are adjusted so that the amplitude of glitches decrease.

The simulations are performed on a 10mm long bus at minimum spacing and minimum width on Metal 2 in CMOS12 TSMC technology. In a typical process case, 10% performance gain can be achieved for the bus structure specified above. On the other hand in a very noisy environment which may occur due to process variations the threshold may be raised by the calibrator and hence avoid glitches at the output of receiver. In this case penalty will have to be paid in terms of increase in worst case delay along the bus. Glitch prevention may be very essential at the output of the receiver, especially in asynchronous circuits.